Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled)

2. (previously presented) The method as recited in claim ~~1~~5, wherein the gate stack structure further includes a diffusion barrier layer in between the polysilicon layer and the metal layer, wherein the dielectric capping layer a silicon oxide-based layer.

3. (original) The method as recited in claim ~~1~~5, wherein the capping layer is made of one of material selected from a group consisting of SiO_2, SiO_xF_y and SiO_xN_y.

4. (canceled)

5. (currently amended) A method for fabricating a transistor with a polymetal gate electrode structure, the method comprising:

forming a gate insulation layer on a substrate;

forming a patterned gate stack structure over the gate insulation layer, wherein the patterned stack structure includes a polysilicon layer as a lower layer and a metal layer as an upper layer;

forming a dielectric capping layer along a profile containing the patterned gate stack structure and on the gate insulation layer at a predetermined temperature that prevents oxidation of the metal layer, the capping layer including a horizontal portion and a vertical portion that together enclose the patterned gate stack structure; and

performing a gate re-oxidation process,

wherein silicon oxide-based the capping layer is formed by performing one of an atomic layer deposition (ALD) technique and a plasma enhanced chemical vapor deposition

(PECVD) technique at a temperature in a range from about 70 °C to about 400 °C, ~~The method as recited in claim 4,~~

wherein the step of forming the silicon oxide-based capping layer through the use of the ALD technique includes the steps of:

loading a wafer containing the patterned gate stack structure into a chamber;

flowing a source gas of silicon (Si) into the chamber and purging the remaining gas; and

flowing a source gas of oxygen into the chamber and purging the remaining gas.

6. (original) The method as recited in claim 5, wherein the silicon source gas is one of silicon hexachloride ($SiCl_6$) or silicon tetrachloride ($SiCl_4$).

7. (previously presented) The method as recited in claim 5, wherein the oxygen source gas is a gas selected from a group consisting of H_2O, O_2, NO and N_2O and a gas obtained by mixing the listed gases, wherein the capping layer has a thickness of no more than about 200 Å.

8. (original) The method as recited in claim 6, wherein the Si source gas is flowed into the chamber as simultaneous as one of pyridine (C_5H_5N) or ammonium (NH_3) gas functioning as a catalyst for lowering a process temperature is flowed thereinto.

9. (original) The method as recited in claim 7, wherein the oxygen source is flowed into the chamber as simultaneous as one of pyridine (C_5H_5N) or ammonium (NH_3) gas functioning as a catalyst for lowering a process temperature is flowed thereinto.

10. (currently amended) The method as recited in claim 5~~1~~, wherein the metal layer is made of one material selected from a group consisting of tungsten (W), molybdenum (Mo), tantalum (Ta), titanium (Ti), ruthenium (Ru), iridium (Ir) and platinum (Pt).

11. (original) The method as recited in claim 2, wherein the diffusion barrier layer is formed with a material selected from a group consisting of WN_x, SiN_x, $TiAl_xN_y$, HfN_x, ZrN_x, TaN_x, TiN_x, AlN_x, $TaSi_xN_y$, $TiAl_xN_y$.

12. (currently amended) The method as recited in claim 5~~1~~, wherein the gate stack structure is formed by stacking a tungsten layer, a tungsten nitride layer and a polysilicon layer.

13. (previously presented) A method for fabricating a semiconductor device with a polymetal gate electrode structure, the method comprising :

forming a gate oxide layer on a substrate;

forming a gate stack structure by sequentially stacking and subsequently etching a polysilicon layer, a diffusion barrier layer, a tungsten layer and a hard mask insulation layer on the gate oxide layer;

forming a silicon oxide layer on a surface of the gate oxide layer exposed by the etching and along a profile containing the gate stack structure by performing an atomic layer deposition (ALD) technique at a predetermined temperature that prevents oxidation of the barrier layer or tungsten layer, or both; and

performing a gate re-oxidation process.

14. (original) The method as recited in claim 13, wherein the silicon oxide layer has a thickness ranging from about 50 Å to about 200 Å.

15. (original) The method as recited in claim 13, wherein the silicon oxide layer is formed by using the ALD technique performed at a temperature ranging from about 70 °C to about 400 °C.

16. (original) The method as recited in claim 13, further comprising the step of carrying out a thermal treatment for densifying the silicon oxide layer and removing impurities contained in the silicon oxide layer after the step of forming the silicon oxide layer.

17. (previously presented) A method for fabricating a semiconductor device, the method comprising :

forming a gate oxide layer on a substrate;

forming a gate stack structure on gate oxide layer, the gate stack structure including a polysilicon layer, a diffusion barrier layer, a metal layer, and a hard mask insulation layer ;

forming a silicon oxide layer along a profile of the gate stack structure at a predetermined temperature that prevents oxidation of the barrier layer or metal layer, or both, the predetermined temperature being no more than about 400 °C, wherein the silicon oxide layer is formed using an atomic layer deposition (ALD) technique; and

performing a gate re-oxidation process after the formation of the silicon oxide layer.

18. (previously presented) The method of claim 17, wherein the silicon oxide layer encloses the gate stack structure.

19. (previously presented) The method of claim 17, wherein the silicon oxide layer is a capping layer that has a thickness of no more than about 200 Å.